Synthesis and Characterization of Ge-related Microstructures and Nanostructures

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Abstract

A large quantity of single crystalline Ge micro and nanostructures have been synthesized by using a simple vapor transport method by using optimizing conditions. It makes possible to synthesize nanowires at relatively low temperature by using the powder source with high evaporation temperature. A systematic study of temperature effect on synthesis of Ge nanowire shows that Ge nanostructures are yielded from 500 °C to 600 °C processing using Ge and GeO_2 powders as the feeding sources, followed by metal-catalytic VLS growth mechanism.

Keywords: Germanium; Microstructure; Nanostructure; VLS growth.

Introduction

Nanoscale one-dimensional (1D) structures have always stimulated great interest due to quantum size effects and novel properties they promise to bring to a wide range of electronic and optoelectronic devices [1], chemical [2] and biological sensors, and photovoltaic systems [3]. Out of that germanium (Ge) is an interesting group IV semiconductor and has been considered for application in high-speed electronics. Ge offers a number of properties that are superior in device applications, e.g., higher carrier mobility, larger exciton radius, lower processing temperatures and thus easier integration with conventional devices [4]. Many synthesis methods for preparation of Ge NWs have been reported, e.g., laser ablation, vapor transport, low temperature chemical vapor deposition (CVD) [5-10]. Among the different synthesis routes for the preparation of Ge nanowires (NWs), thermal evaporation is particularly interesting as it is a simple way of producing large quantities of Ge NWs [5, 9]. Growth temperature is one of the most important factors in NW-based electronics. It impacts not only the physical properties of NWs, such as morphology and crystal structure, but also the integration of NW devices. In present work, a thermal evaporation system was used to synthesize Ge nanostructures. The growth of Ge nanostructures was investigated by varying parameters like sources used for growth, growth temperature and pressure of carrier gas.

Experimental Work

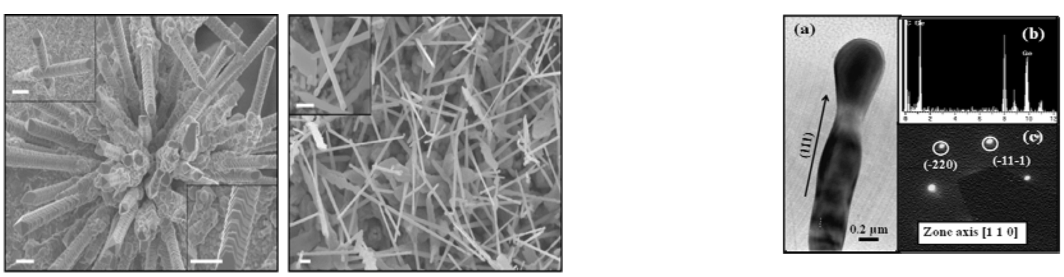
The germanium (Ge) microstructures were observed at 550 °C without using catalysis. P-type silicon

(001) wafer was ultrasonically cleaned in ethanol for 10 min. and utilized for experiment. The Ge microtowers, and microwires were grown by a vapor transport method using a three zone furnace. A mixture of commercial Ge (99.999 %, Alfa Aesar), GeO_2 (99.999 %, Alfa Aesar) was used to synthesize Ge microtowers, and microwires with a 1:1 and 1:3 ratios respectively, with substrate temperature of 500 ^{0}C. The mixture was placed in an alumina boat, which was heated to a peak temperature of 1100 ^{o}C in zone - I. The silicon wafers without catalysis were placed in zone - II and zone - III at 500 ^{o}C. The samples were heated to 1100 ^{o}C at a rate of 20 ^{o}C /min. with the reaction time of 60 min. and with a 60 sccm Ar flowing through the tube. The Ge nanowires sheathed with oxide layer and single crystalline Ge nanowires were grown by a vapor transport method using Ge and GeO_2 powders with a 1:3 ratio with a substrate temperature of 500 and 600 ^{o}C respectively. The silicon wafer with 2-nm thick gold film deposited on it was used as a substrate.

Results and Discussions

Figure 1(I) depicts field emission scanning electron microscopy (FESEM) image of tower like structure. The stacking layers were observed from the inset of FESEM image of Figure 1(I).

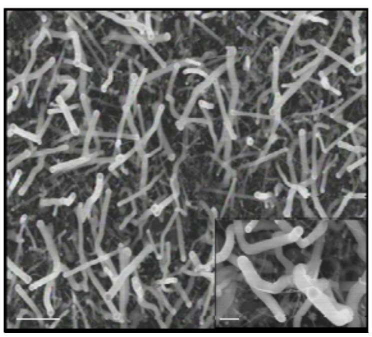
Bunches of tower like structure was observed on the silicon wafer. The diameter and length of the tower like structure was in the range of 8 - 10 μm and 70 - 80 μm respectively. With the same experimental parameters as that of microtowers except the source ratio i.e. 1:3, Ge:GeO_2 powders in this experiment the high density of wire like structures were observed as shown in Figure 1(II). Inset of the FESEM images shows that at the tip part of the wires bead like structure was formed. The diameter and length of the wires were in the range of 400 - 500 nm and 10 - 15 μm respectively. Inset of Figure 1(II) depicts as TEM image [inset (a) of Figure 1(III)] of wire morphology, which contains bead like structure at the tip of the microwire. The diameter of the microwire from the TEM image is found to be ~ 400 nm. The diameter variation from top to bottom was observed with the variation of contrast in TEM image.



(i) (ii) (iii)

Figure 1. (I) FESEM image of Ge micro -towers. (inset - magnified microtower parts, scale bar = 10 μm), (II) FESEM image of Ge microwires. (inset- magnified FESEM image, scale bar = 1 μm). (III) (a) TEM image for inset of (II) (scale bar = 200 nm) of nanowire structure corresponding (b) EDS spectrum and (c) SAED pattern.

The EDS [inset (b) of Figure 1(III)] analysis confirmed that the microwire consists of Ge. Clearly, the SAED pattern [inset (c) of Figure 1(III)] revealed that the growth direction of Ge microwire is (111) with [110] zone axis. As the final aim of the experiments was to synthesis the single crystalline Ge nanowires with small diameter and long length i.e. with high aspect ratio, it was essential to tune the experimental parameters. But to tune the diameter of the Ge nanowires in a controlled way, 2 nm gold coated silicon wafer was used as a substrate. At the substrate temperature of 500 ^{o}C, the high density of nanowires was obtained as shown in FESEM image in Figure 2(I). The inset is corresponding magnified image of nanowires. The diameter and length of the nanowires are in the range of 60 - 100 nm and 5 µm respectively. Figure 2(II) depicts a TEM image and shows the oxide sheathed layer around nanowire. The diameter of the nanowire from the TEM image is found to be ~ 60 nm. The thickness of the oxide layer around Ge nanowires is about 5 - 10 nm. The EDS spectra shows Ge and Ge oxide contents at core [Figure 2(II) b] and shell [Figure 2(II) c] respectively.



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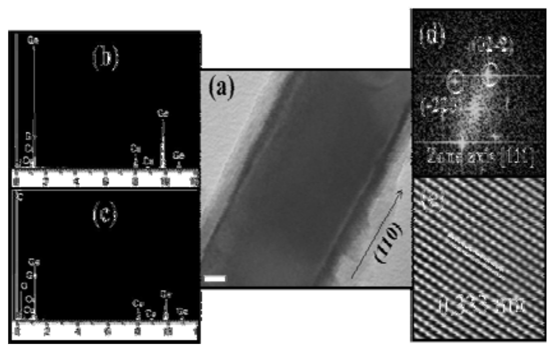

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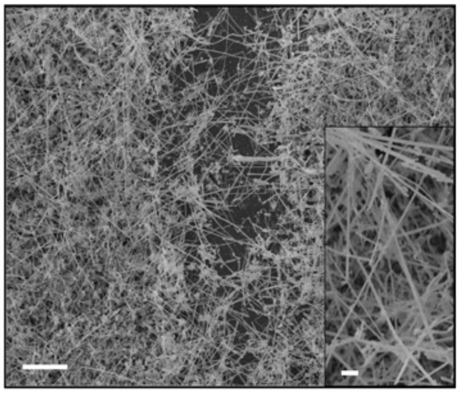
Figure 2. (I) FESEM image of Ge nanowires and inset is corresponding magnified image. The scale bars for low magnified and high magnified images are 1 µm and 100 nm respectively. (II) (a) TEM image of the Ge nanowire sheathed with oxide layer, (b and c) EDS pattern of core and shell of the nanowire respectively, (d) corresponding SAED pattern and (e) HR image (scale bar = 10 nm).

Clearly, the SAED pattern and HRTEM image [zone axis - [111], d spacing - 0.333 nm] revealed that, the nanowire consists of Ge and the growth direction of oxide layer sheathed Ge nanowire is [111]. In a similar way, by using same experimental parameters and at the substrate temperature of 600 ^{o}C, the high density of single crystal nanowires was obtained as shown in FESEM image in Figure 3(I). The diameter and length of the nanowires was in the range of 50 - 60 nm and 5 - 10 µm respectively, as observed from the low and high magnified [inset of Figure 3(I)] images. Figure 3(II) depicts a TEM image of the nanowire structure.

The TEM image revealed the uniformity of the nanowire and absence of oxide layer or particle. The EDS [Figure 3(II) b] analysis confirmed that the nanowire consists of pure Ge. The diameter of the nanowire from the TEM image is about ~ 60 nm. The SAED pattern and HRTEM image [zone axis -

[110], d spacing - 0.335 nm] revealed that the nanowire consists of Ge. The growth direction of Ge nanowire with oxide particle is [111]. Thus the single crystalline uniform germanium nanowires were grown successfully.



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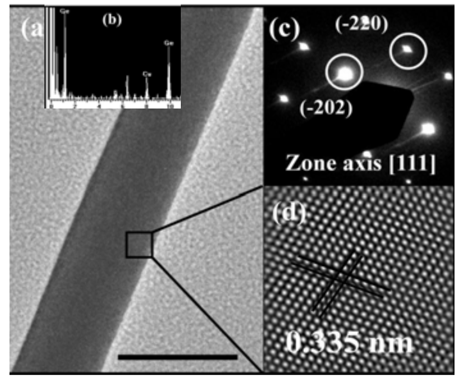

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Figure 3. (I) FESEM image of Ge nanowires (inset - magnified image). The scale bars of low and high magnified images are 1 µm and 100 nm respectively. (II) (a) TEM image of Ge nanowire and corresponding (b) EDS spectrum, (c) SAED pattern and (d) HR image (scale bar = 100 nm).

Conclusions

The variation in experimental parameters such as source amount and substrate temperature can play vital role in formation of different morphological changes of germanium nanowires. In conclusion, a simple vapor transport has been employed to synthesize single crystalline germanium nanowires with high yield and high purity, so that it can be utilized for electronic and optical applications in a large scale.

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